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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Andrew M. Welin

Art Unit: Not Assigned

Serial No.: 09/785,768

Examiner: Not Assigned

Filed: 02/16/01

Docket: TI-29045

For: Systems, Processes and Integrated Circuits for Improved Packet Scheduling of Media Over Packet

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that the above correspondence is being deposited with the U.S Postal Service as First Class Mail in an envelope addressed to. Assistant Commissioner for Patents Application Processing Division's Customer Correction Branch, Washington, D.C. 20231.

Karen Vertz 3-14-01
Karen Vertz Date

Assistant Commissioner for
Patents
Washington, D. C. 20231

PRELIMINARY AMENDMENT

Dear Sir:

Prior to the examination of the above identified application, please amend as follows:

IN THE CLAIMS:

Add the following new claims:

131. An electronic system comprising:

a processor circuit;

an egress packet control having stored instructions that generate for first and second received packets respective deadline intervals and order the processing in the processor circuit of the first and second received packets according to the respective deadline intervals; and

a printed wiring assembly bearing the processor circuit and the egress packet control.

132. An electronic system as claimed in claim 131 wherein the egress packet control defines the deadline interval Dj for an arriving packet j, having a sequence number Sj and frame width F, from a deadline Di of an earlier packet i having a sequence number Si, substantially as a function of frame width F and the difference of sequence numbers Sj and Si.

133. An electronic system as claimed in claim 131 wherein the egress packet control has stored instructions to preempt processing of the first received packet by preemptively processing the second received packet, when the deadline interval for the second received packet is less than the deadline interval respective to the first received packet by a predetermined amount.

134. An electronic system as claimed in claim 131 wherein the egress packet control has stored instructions for ingress packet processing, and for preempting egress packet processing of an egress packet having a deadline interval exceeding a value, by preemptively executing ingress packet processing of at least one ingress packet.

135. An electronic system as claimed in claim 131 having channel decoders that operate on non-coincident frame boundaries, and wherein if the second packet has a second deadline earlier than the first deadline, the egress packet control has stored instructions for testing to determine whether both the second and first packets can be decoded ahead of their respective deadlines, and if so, then preemptively executing decode of the second packet.

136. An electronic system as claimed in claim 131 whereas the egress packet control has stored instructions for the computing for each of said received packets respective deadline intervals as circular time differences between a respective deadline D and a respective packet arrival time A.

Should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

Respectfully submitted,

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